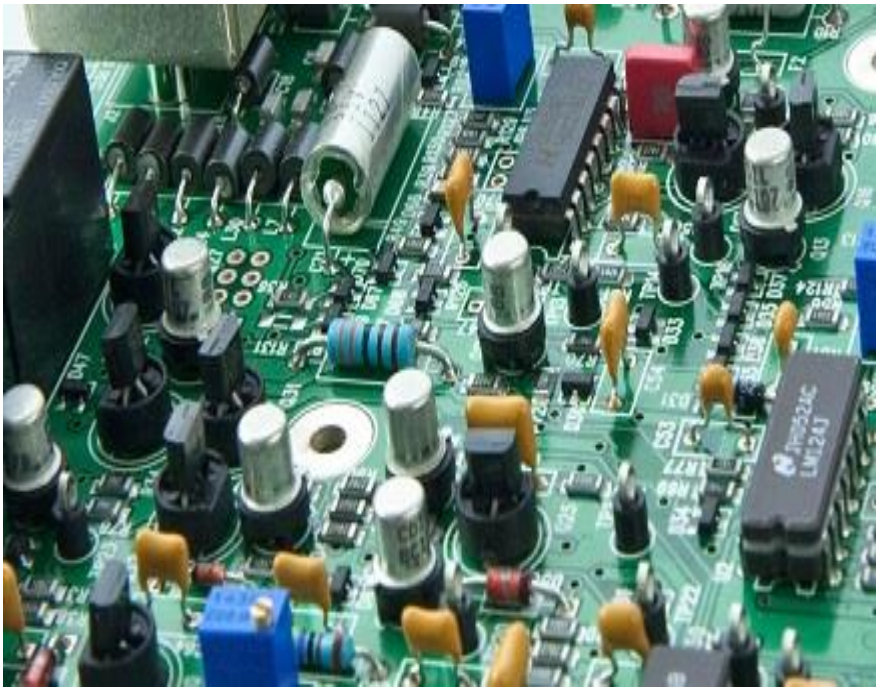

ANALOG ELECTRONICS LABORATORY (EI181313)MANUAL

ELECTRICAL ENGINEERING DEPARTMENT JORHAT ENGINEERING COLLEGE

The PEO - Program Educational Objectives of Electrical Engineering Graduate Program are
The graduates of Electrical Engineering Program of Jorhat Engineering College will be to

1. Create professionals who can pursue good career in academia, industry and societal institutions.
2. Motivate for continuing higher studies in Electrical Engineering and its allied domains

PO-Program Outcomes:

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics, responsibilities, and norms of the engineering practice.
9. **Individual and teamwork**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PSO - Program Specific Outcomes of Electrical Engineering Graduate Program:

The graduates of Electrical Engineering Program of Jorhat Engineering College will be able to

1. Develop electrical power and drive system to meet desired needs of academia and industry.
2. Design electronic systems to ease real life problems of academia, industry and society.

Course Objectives:

- To examine characteristics and application of diode, BJT, FET.
- To analyse linear and non-linear applications of OP-AMP.

Course Outcomes:

CO1: To analyse characteristics and application of semiconductor devices**.**

CO2: To examine linear and non-linear application of OP-AMP.

CO3: To analyse application of 555-IC timer and DAC.

Evaluation Scheme for Lab. Internals and Externals

Internal:

Evaluation Criteria	Marks
Journal	5
Lab. Quiz Test	10
TOTAL	**15**

External:

Lab. Evaluation Criteria	Marks
Circuit Diagram of Experiment	5
Experiment Procedure	5
Viva	10
Results & Calculation	5
Theory	5
Experiment Connection	5
Total	**35**

Quiz Test:

A quiz test is conducted online through Google classroom based on the Lab experiments for internal assessment. Quiz test was of MCQ types.

CONTENTS

EXPERIMENT NO.1

AIM OF THE EXPERIMENT: To study the characteristics of PN diode and determine the static and dynamic resistances from it.

APPARATUS REQUIRED:

Sl.No.	Name of the apparatus	Specification	Quantity
1.	Semiconductor devices trainer	Model DS-373	1
2.	Patch cords	4mm cords	As per requirement
3.	Voltmeter	(0-5) V, (0-50) V PMMC type	1
4.	Ammeter	(0-25) mA, (0-250) µA PMMC type	1

CIRCUIT DIAGRAM:

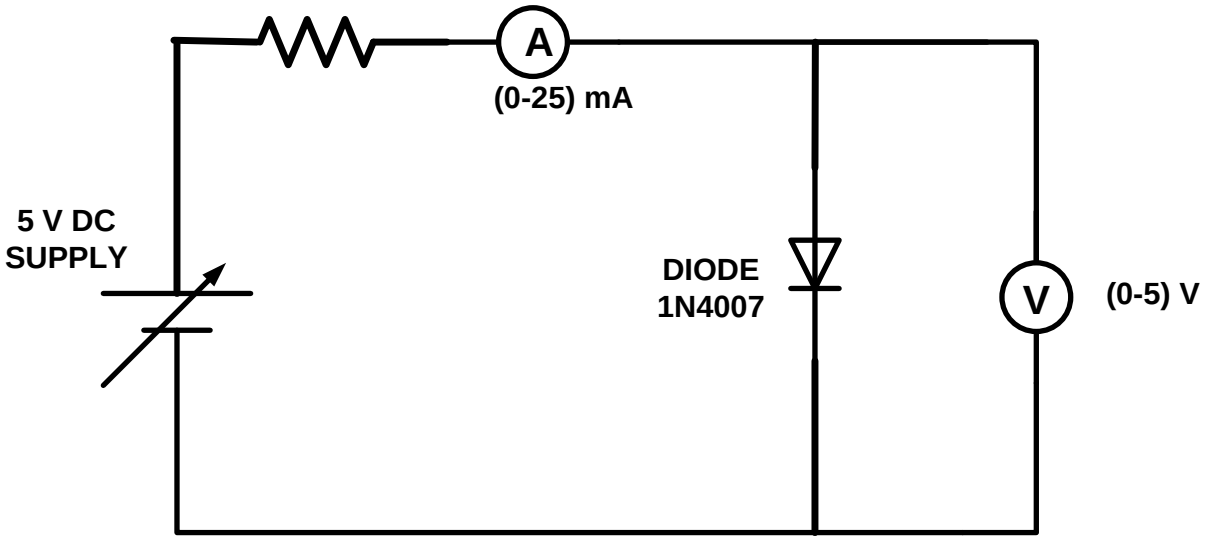

Fig.1.1(Forward characteristics of diode)

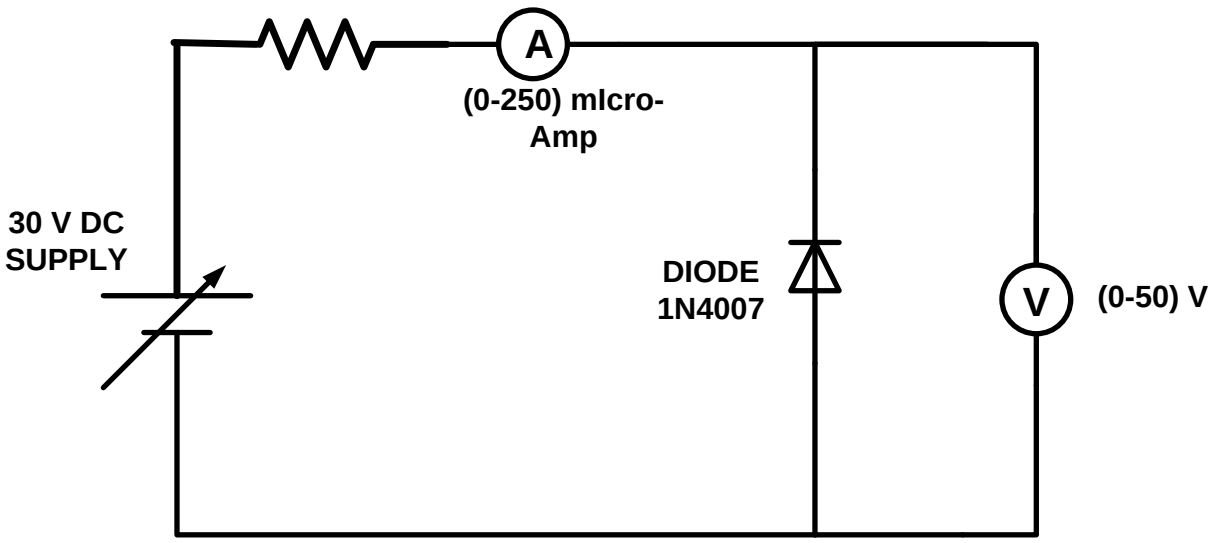

Fig. 1.2 (Reverse characteristics of diode)

THEORY: The P-N junction supports uni-directional current flow. If +ve terminal of the input supply is connected to Pside and –ve terminal is connected the n side, then diode is said to be forward biased condition. In this condition the height of the potential barrier at the junction is lowered by an amount equal to given forward biasing voltage. Both the holes from p-side and electrons from n-side cross the junction simultaneously thereby decreasing the depleted region. This constitutes a forward current (majority carrier movement – diffusion current). Assuming current flowing through the diode to be very large, the diode can be approximated as short circuited switch. Diode offers a very small resistance called forward resistance (few ohms) Reverse bias operation If negative terminal of the input supply is connected to p-side and –ve terminal is connected to n-side then the diode is said to be reverse biased. In this condition an amount equal to reverse biasing voltage increases the height of the potential barrier at the junction. Both the holes on P-side and electrons on N-side tend to move away from the junction there by increasing the depleted region. However, the process cannot continue indefinitely, thus a small current called reverse saturation current continues to flow in the diode. This current is negligible; the diode can be approximated as an open circuited switch it offers a very high resistance called reverse resistance (few kilo-ohms).

Static Resistance: The opposition offered by a diode to the direct current flowing forward bias condition is known as its DC forward resistance or Static Resistance. It is measured by taking the ratio of DC voltage across the diode to the DC current flowing through it at an operating point. **Dynamic Resistance**: The opposition offered by a diode to the changing current flow I forward bias condition is known as its AC Forward Resistance. It is measured by a ratio of change in voltage across the diode to the resulting change in current through it for an operating point P. **Average Resistance:** Same as dynamic resistance but measured between extremities. Diode current equation.

The volt-ampere characteristics of a diode explained by the following equations:

$$I = I_0 * \exp(\frac{V}{\eta V_T} - 1)$$

Where I = current flowing in the diode, I_0 = reverse saturation current V = voltage applied to the diode, V_T = volt- equivalent of temperature = kT/q = T/ 11,600 = 26mV (at room temp) =1 (for Ge) and 2 (for Si)

PROCEDURE:

Forward Bias:

- Connect the circuit as shown in Fig.1 (PN Junction diode with milli-ammeter in series with the diode).
- Initially vary Regulated Power Supply (RPS) voltage Vs in steps of 0.1 V. Once the current starts increasing vary Vs in steps of 0.02V and note down the corresponding readings V_D and I_D.
- Tabulate different forward currents obtained for different forward voltages.
- Plot the V-I characteristics and calculate the resistance levels
- Compare the theoretical and practical values (cut-in voltage and resistances).

Reverse Bias:

- Connect the circuit as shown in Fig.2 (Point contact diode in series with micro ammeter).
- Vary Vs in the Regulated Power Supply (RPS) gradually in steps of 1V from 0V to 12V and note down the corresponding readings V_D and I_D.
- Tabulate different reverse currents obtained for different reverse voltages.
- Plot the V-I characteristics and calculate the resistance levels
- Compare the theoretical and practical values.

TABULATION:

Forward Bias:

Sl.No.	V_D in Volt	I_D in mA
1.		
2.		
3.		
4.		
5.		
6.		
7.		
8.		
9.		

10.		

Reverse Bias:

Sl.No.	V_D in Volt	I_D in mA
1.		
2.		
3.		
4.		
5.		
6.		
7.		
8.		
9.		
10.		

MODEL GRAPH:

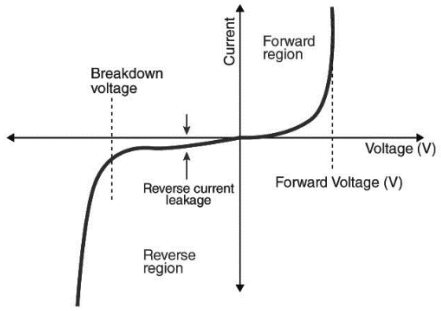

Fig. 1.3 I-V characteristics of diode

CALCULATION:

Calculate static resistances of diode in forward and reverse bias condition from the characteristics plotted.

CONCLUSION:

DISCUSSION QUESTIONS:

1. Why does semiconductor device possess negative resistance?
2. Which one is greater between forward resistance and reverse resistance and why?
3. Explain forward break down voltage of a diode.
4. What is Schockley's equation?
5. Explain Thermal Voltage of diode.

EXPERIMENT NO.2

AIM OF THE EXPERIMENT: To study half wave and full wave rectifier and to calculate rectification efficiency and Transformer Utilization Factor.

APPARATUS REQUIRED:

Sl.No.	Name of the apparatus	Specification	Quantity
1.	AC Wave Shaping Trainer Kit	Model DS-348	1
2.	Patch cords	4mm cords	As per requirement
3.	DSO	DSO1052B, 50MHz, 1GSa/S	1
4.	Probes	T5060,60 MHz/6MHz, 10X:600Vpk, 1X:200Vpk, CAT-II	2

CIRCUIT DIAGRAM:

Half Wave Rectifier:

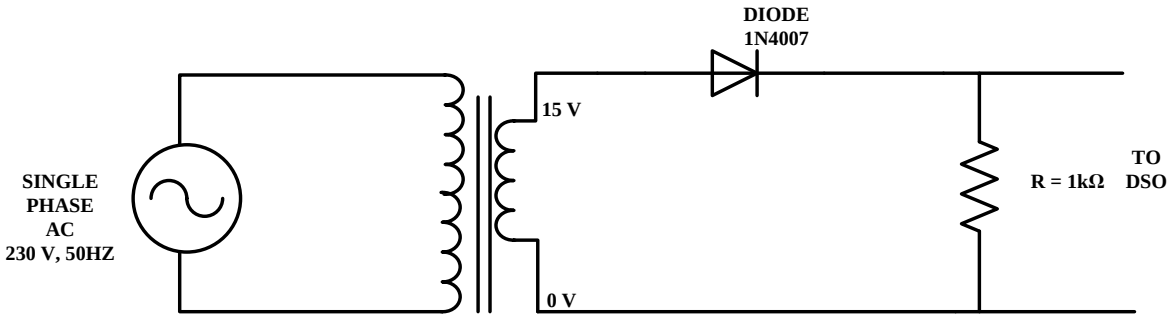

Fig. 2.1 Half wave rectifier

Full Wave Rectifier:

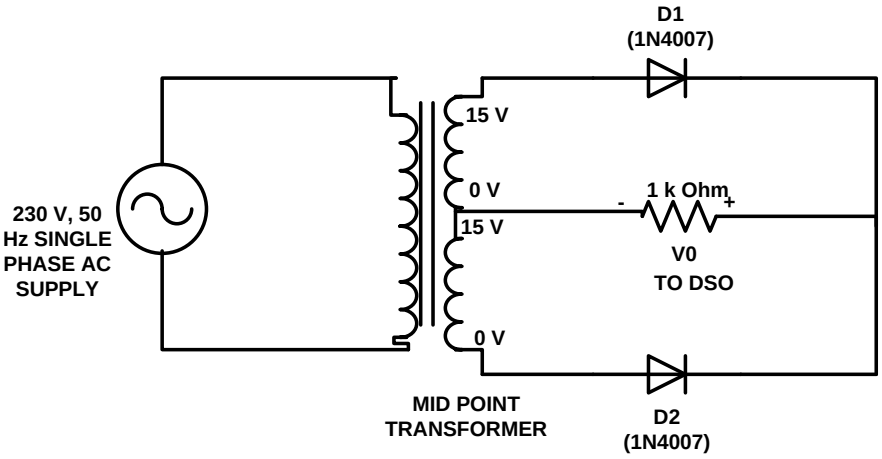

Fig. 2.2 Full Wave Rectifier

THEORY: A rectifier is a circuit that converts a pure AC signal into a pulsating DC signal or a signal that is a combination of AC and DC components. A half wave rectifier makes use of single diode to carry out this conversion (Fig.2.1) . It is named so as the conversion occurs for half input signal cycle. During the positive half cycle, the diode is forward biased and it conducts and hence a current flows through the load resistor. During the negative half cycle, the diode is reverse biased and it is equivalent to an open circuit, hence the current through the load resistance is zero. Thus the diode conducts only for one half cycle and results in a half wave rectified output. A full wave rectifier makes use of a two diodes to carry out this conversion(Fig 2.2). It is named so as the conversion occurs for complete input signal cycle. The full-wave rectifier consists of a center-tap transformer, which results in equal voltages above and below the center-tap. During the positive half cycle, a positive voltage appears at the anode of D1 while a negative voltage appears at the anode of D2. Due to this diode D1 is forward biased it results in a current Id1 through the load R. During the negative half cycle, a positive voltage appears at the anode of D2 and hence it is forward biased. Resulting in a current Id2 through the load at the same instant a negative voltage appears at the anode of D1 thus reverse biasing it and hence it doesn't conduct.

Percentage of Regulation:

It is a measure of the variation of AC output voltage as a function of DC output voltage.

Percentage of regulation = $\left(\frac{V_{NL} - V_{FL}}{V_{FL}}\right) * 100$ %

V_{NL} = Voltage across load resistance, when minimum current flows through it.

V_{FL} = Voltage across load resistance, when maximum current flows through.

For an ideal rectifier, the percentage regulation is 0 percent. The percentage of regulation is very small for a practical half wave and full wave rectifier.

Peak- Inverse – Voltage (PIV):

It is the maximum voltage that has to be with stood by a diode when it is reverse biased

$PIV_{HWR} = Vm$ $PIV_{FWR} = 2Vm$

Comparison of Half-wave and Full-wave rectifier

S. No.	Particulars	Type of Rectifier	
		Half-Wave	Full-Wave
1.	No. of diodes	1	2
2.	Maximum Rectification Efficiency	40.6%	81.2%
3.	$V_{d.c}$ (no load)	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$
4.	Ripple Factor	1.21	0.48
5.	Peak Inverse Voltage	V_m	$2V_m$
6.	Output Frequency	f	2f
7.	Transformer Utilization Factor	0.287	0.693

Ripple Factor:

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol 'γ'.

$$\gamma_{HWR} = \frac{V_{AC}}{V_{DC}} = 1.21 \qquad \gamma_{FWR} = \frac{V_{AC}}{V_{DC}} = 0.48$$

Rectification Factor:

The ratio of output DC power to input AC power is defined as efficiency.

$$\eta = \frac{(V_{DC})^2}{(V_{AC})^2} \qquad \eta_{HWR} = 40.6\% \qquad \eta_{FWR} = 81\%$$

PROCEDURE:

- Connect as per the circuit diagram.
- Connect two channels of DSO to the input and output of the rectifier respectively.
- Compute ripple factor, Transformer utilization factor, rectification efficiency by using the formula and compare it with those of full wave rectifier.

CALCULATION:

Calculate the performance parameters of half wave and full wave rectifier.

CONCLUSION:

DISCUSSION QUESTIONS:

1. Explain PIV rating of diode.
2. Explain the role of filters in rectifier circuits.
3. Explain Transformer Utilization Factor of rectifiers.
4. Cite the reason of low rectification efficiency of rectifiers.
5. Compare the rating of diode that can be used in half wave rectifier to full wave mid-point transformer.

EXPERIMENT NO.3

AIM OF THE EXPERIMENT: To study the input and output characteristics of a BJT common base mode.

APPARATUS REQUIRED:

Sl.No.	Name of the apparatus	Specification	Quantity
1.	Transistor Characteristics Module	Model DS-373	1
2.	Patch cords	4mm cords	As per requirement

CIRCUIT DIAGRAM:

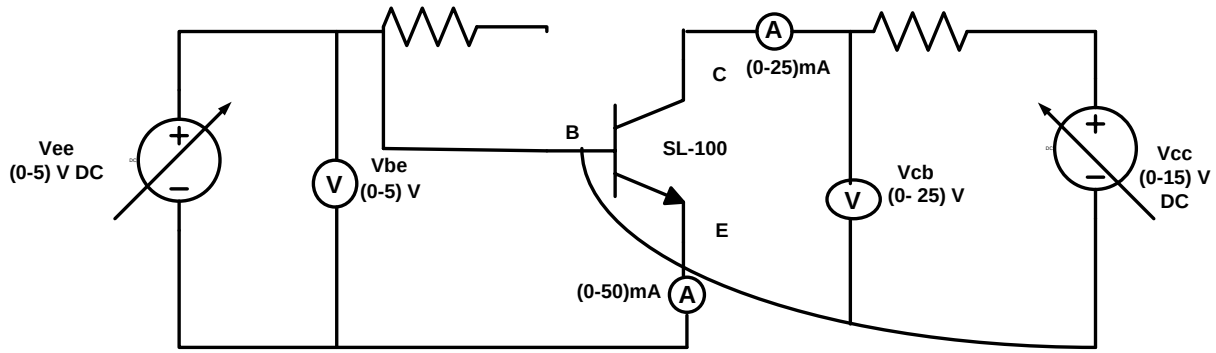

Fig. 3.1 BJT in Common Base mode

THEORY:

The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential. Throughout this text all current directions will refer to conventional (hole) flow rather than electron flow. The result is that the arrows in all electronic symbols have a direction defined by this convention. Recall that the arrow in the diode symbol defined the direction of conduction for conventional current.

In the active region the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased and in saturation mode both the junctions are forward biased.

The input characteristics of BJT is plotted between the input base current I_E vs V_{BE} for different values of output voltage V_{CE}. The output characteristics of BJT is plotted between output current I_C vs V_{CE} for different values of emitter current I_E.

PROCEDURE:

Input Characteristics:

- Connect as per the circuit diagram.
- Get the connection checked by lab instructor or course instructor.
- Keep all the variable potentiometer in the zero position.
- Switch on the power to the kit.
- Keep the V_{CC} potentiometer to a value 1 V (say)
- Now vary the potentiometer of V_{EE} to 1 V in a step of 0.1 V each.
- Note down the readings of voltmeter and ammeter showing V_{BE} and I_E respectively as given in the tabulation below.
- Increase the V_{CC} potentiometer value to a value 2 V and so on.
- Take at least 10 readings.
- Draw the characteristics I_E (X-axis) vs V_{EB} (Y-axis).

Output Characteristics:

- Connect as per the circuit diagram.
- Get the connection checked by lab instructor or course instructor.
- Keep all the variable potentiometer in the zero position.
- Switch on the power to the kit.
- Keep the V_{EE} potentiometer to a value so that I_E will be 10 mA (say)
- Now vary the potentiometer of V_{CC} to 1 V in a step of 0.1 V each.
- Note down the readings of voltmeter and ammeter showing V_{CB} and I_C respectively as given in the tabulation below.
- Increase the I_E value to 20 mA.
- Take at least 10 readings.
- Draw the characteristics I_C (X-axis) vs V_{CB} (Y-axis).

TABULATION:

Input Characteristics:

Sl. No.	**V_{CB} = 1.0 V**		**V_{CB} = 2.0 V**		**V_{CB} = 3.0 V**	
	V_{EB} in Volts	**I_E in mA**	**V_{EB} in Volts**	**I_E in mA**	**V_{EB} in Volts**	**I_E in mA**
1.						
2.						
3.						
4.						
5.						
6.						

7.						
8.						
9.						
10.						

Output Characteristics:

Sl. No.	I_E = 10 mA		I_E = 20 mA		I_E = 30 mA	
	V_{CB} in Volts	I_C in mA	V_{CB} in Volts	I_C in mA	V_{CB} in Volts	I_C in mA
1.						
2.						
3.						
4.						
5.						
6.						
7.						
8.						
9.						
10.						

MODEL GRAPH:

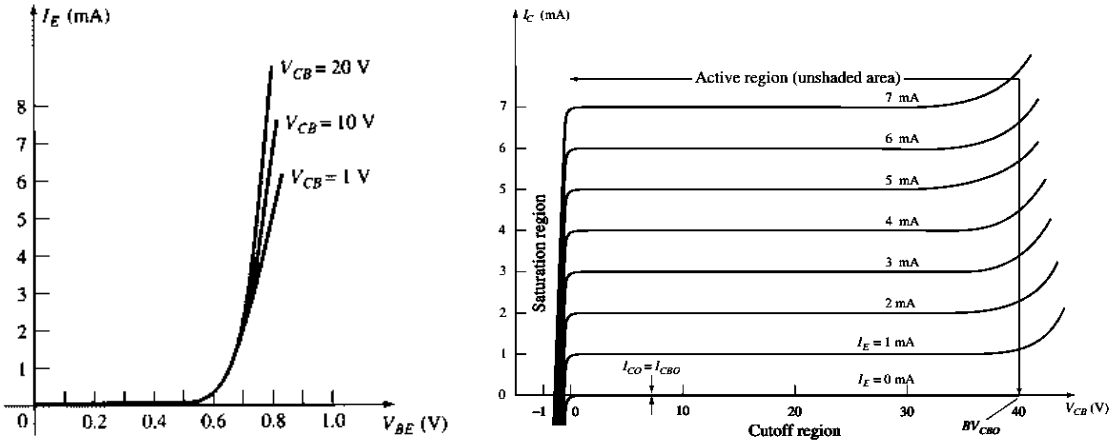

Fig. 3.2 Input and Output Characteristics of BJT in CB mode

CALCULATION:

Determine current amplification factor α for the transistor from the characteristics curve.

CONCLUSION:

DISCUSSION QUESTIONS:

1. Explain current amplification factor for common base configuration.
2. Why is BJT called as bipolar?
3. Why base current is so low?
4. What is the maximum value of V_{CE} of SL100?
5. Explain doping process.

EXPERIMENT NO.4

AIM OF THE EXPERIMENT: To study the input and output characteristics of a BJT common emitter mode.

APPARATUS REQUIRED:

Sl.No.	Name of the apparatus	Specification	Quantity
1.	Transistor Characteristics Module	Model DS-373	1
2.	Patch cords	4mm cords	As per requirement

CIRCUIT DIAGRAM:

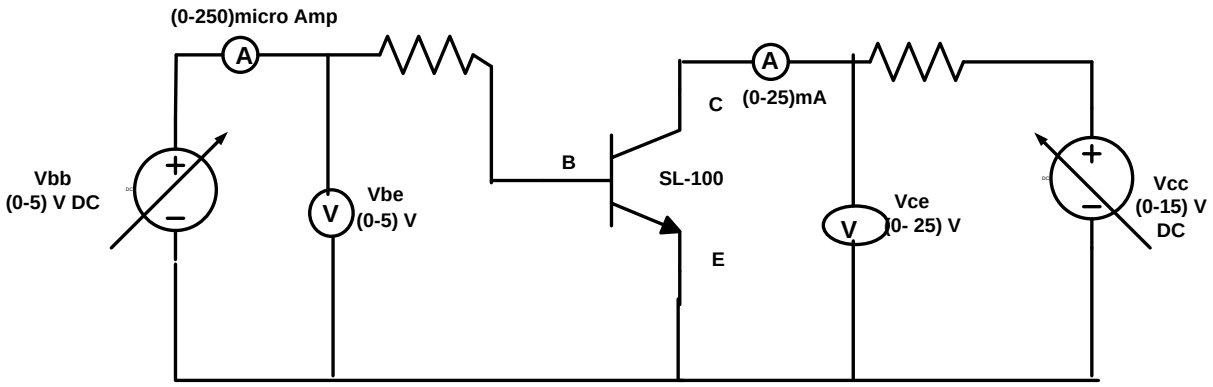

Fig. 4.1 BJT in Common Emitter mode

THEORY: The most frequently encountered transistor configuration appears is called the common-emitter configuration because the emitter is common to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the input or base–emitter circuit and one for the output or collector–emitter circuit. The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input

voltage (V_{BE}) for a range of values of output voltage (V_{CE}). To be noted the magnitude of I_B is in microamperes, compared to mill amperes of I_C. Consider also that the curves of I_B are not as horizontal as those obtained for I_E in the common-base configuration, indicating that the collector-to emitter voltage will influence the magnitude of the collector current. The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for I_B are nearly straight and equally spaced. In F this region exists to the right of the vertical dashed line at V_{CEsat} and above the curve for I_B equal to zero. The region to the left of V_{CEsat} is called the saturation region. In the active region of a common-emitter amplifier, the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.

PROCEDURE:

Input Characteristics:

- Connect as per the circuit diagram.
- Get the connection checked by lab instructor or course instructor.
- Keep all the variable potentiometer in the zero position.
- Switch on the power to the kit.
- Keep the V_{CC} potentiometer to a value 1 V (say)
- Now vary the potentiometer of V_{BB} to 1 V in a step of 0.1 V each.
- Note down the readings of voltmeter and ammeter showing V_{BE} and I_B respectively as given in the tabulation below.
- Increase the V_{CC} potentiometer value to a value 2 V and so on.
- Take at least 10 readings.
- Draw the characteristics I_B (X-axis) vs V_{BE} (Y-axis).

Output Characteristics:

- Connect as per the circuit diagram.
- Get the connection checked by lab instructor or course instructor.
- Keep all the variable potentiometer in the zero position.
- Switch on the power to the kit.
- Keep the V_{BB} potentiometer to a value so that I_B will be 50 µA (say)
- Now vary the potentiometer of V_{CC} to 1 V in a step of 0.1 V each.
- Note down the readings of voltmeter and ammeter showing V_{CB} and I_C respectively as given in the tabulation below.
- Increase the I_B value to 100 µA.
- Take at least 10 readings.
- Draw the characteristics I_C (X-axis) vs V_{CE} (Y-axis).

TABULATION:

Input Characteristics:

Sl. No.	V_{CE} = 1.0 V		V_{CE} = 2.0 V		V_{CE} = 3.0 V	
	V_{BE} in Volts	I_B in µA	V_{BE} in Volts	I_B in µA	V_{BE} in Volts	I_B in µA
1.						
2.						
3.						
4.						
5.						
6.						
7.						
8.						
9.						
10.						

Output Characteristics:

Sl. No.	I_B = 50 µA		I_B = 100 µA		I_B = 150 µA	
	V_{CE} in Volts	I_C in mA	V_{CE} in Volts	I_C in mA	V_{CE} in Volts	I_C in mA
1.						
2.						
3.						
4.						
5.						
6.						
7.						
8.						
9.						
10.						

MODEL GRAPH:

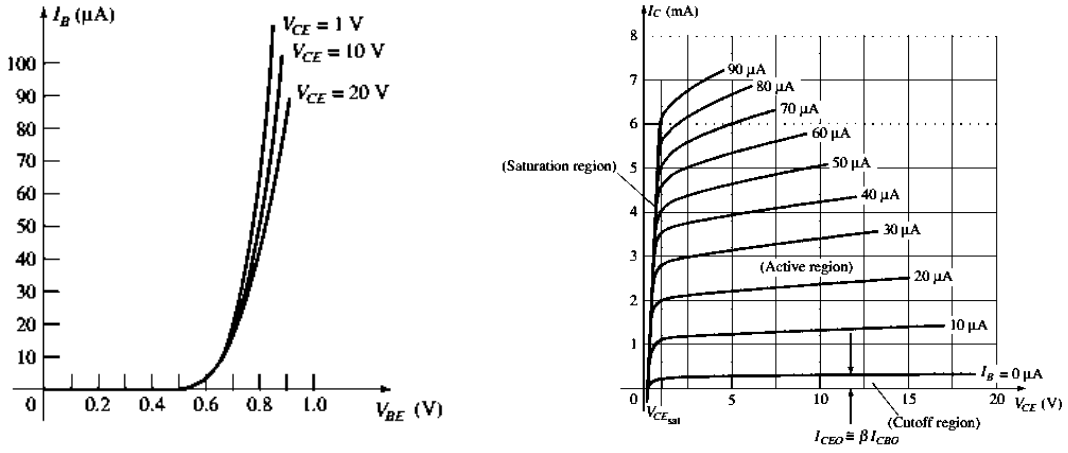

Fig. 4.2 Input and Output Characteristics of BJT in CE mode

CALCULATION:

Determine current amplification factor β for the transistor from the characteristics curve.

CONCLUSION:

DISCUSSION QUESTIONS:

1. Explain current amplification factor for common emitter configuration.
2. Why is BJT called as bipolar?
3. Why base current is so low?
4. Where is Common Emitter configuration used mostly?
5. Explain doping process.

EXPERIMENT NO.5

AIM OF THE EXPERIMENT: To study differentiator and integrator circuit based on OP-AMP

APPARATUS REQUIRED:

Sl.No.	Name of the apparatus	Specification	Quantity
1.	Analog Lab Trainer	Model DS-354	1
2.	Op-Amp module kit	ADT-030	1
3.	DSO	DSO1052B, 50MHz, 1GSa/S	1
4.	Probes	T5060,60 MHz/6MHz, 10X:600Vpk, 1X:200Vpk, CAT-II	2
5.	Patch cords	4mm cords	As per requirement

CIRCUIT DIAGRAM:

Integrator:

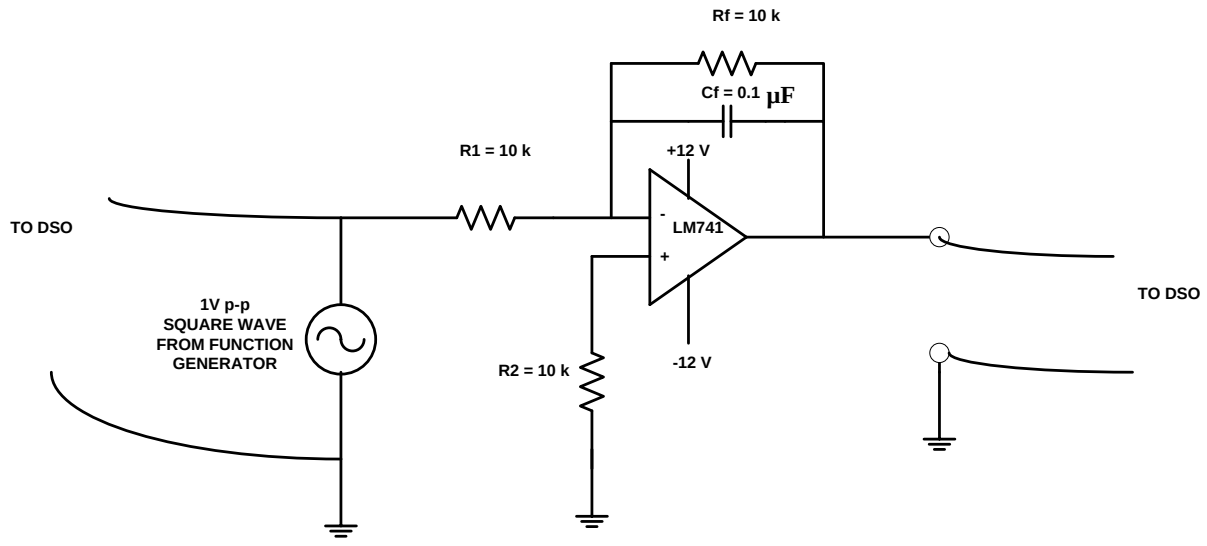

Fig. 5.1 Integrator Circuit Using OP-AMP

Differentiator:

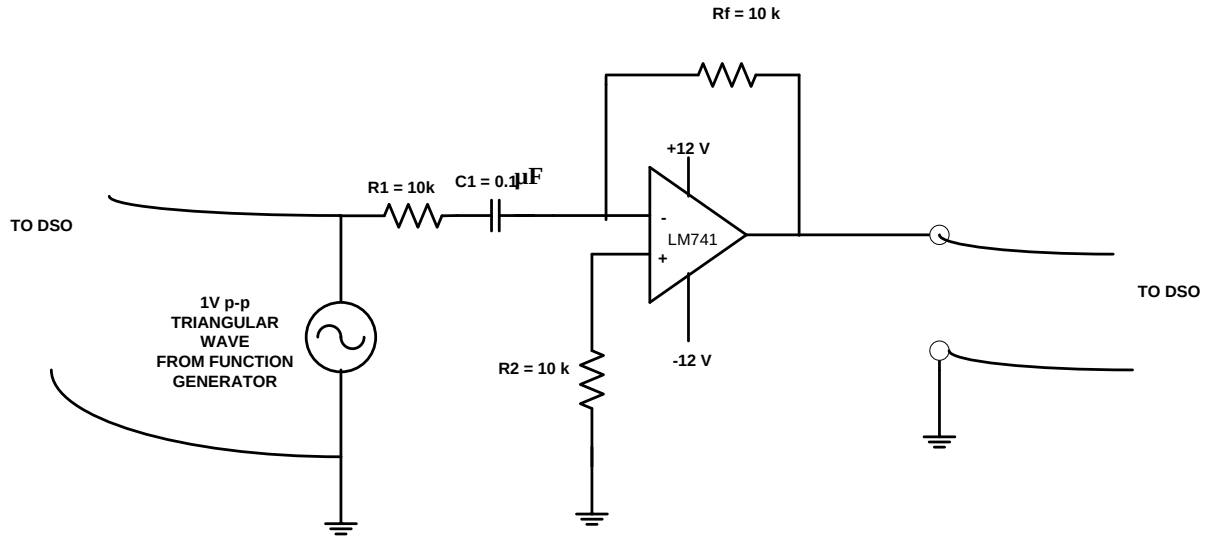

Fig. 5.2 Differentiator Circuit Using OP-AMP

THEORY: If the feedback component used is a capacitor, the resulting connection is called an integrator. The virtual-ground equivalent circuit shows that an expression for the voltage between input and output can be derived in terms of the current I from input to output. Recall that virtual ground means that we can consider the voltage at the junction of Rand X_C to be ground (since Vi = 0 V) but that no current goes into ground at that point.

$$v_o(t) = -\frac{1}{RC}\int v_1(t)\,dt$$

A differentiator circuit, although it is not as useful as the circuit forms covered above, the differentiator does provide a useful operation, the resulting relation for the circuit being

$$v_o(t) = -RC\frac{dv_1(t)}{dt}$$

PROCEDURE:

Integrator:

- Connect integrator as per the circuit diagram.
- Connect a square wave from the function generator to the input of integrator module having amplitude 1V p-p.
- Observe the output in a DSO.
- Note down the magnitude of input voltage and output voltage from the DSO.
- Calculate the voltage gain.
- Vary the frequency of square wave from function generator.
- Compute the voltage gain in each case in decibel(dB)

Differentiator:

- Connect differentiator as per the circuit diagram.
- Connect a triangular wave from the function generator to the input of differentiator module having amplitude 1V p-p.
- Observe the output in a DSO.
- Note down the magnitude of input voltage and output voltage from the DSO.
- Calculate the voltage gain.
- Vary the frequency of triangular wave from function generator.
- Compute the voltage gain in each case in decibel(dB).

TABULATION:

Integrator:

Sl. No.	**V_{in} in Volt**	**V_{out} in Volt**	**Frequency in kHz**	**Voltage Gain**	**Gain in (dB) = 20log(V_{out}/ V_{in})**

Differentiator:

Sl. No.	**V_{in} in Volt**	**V_{out} in Volt**	**Frequency in kHz**	**Voltage Gain**	**Gain in (dB) = 20log(V_{out}/ V_{in})**

CONCLUSION:

DISCUSSION QUESTIONS:

1. Explain offset voltage of Op-Amp.
2. Cite practical applications of Integrator and differentiator?
3. Can a differentiator or integrator be made by taking only R, L, and C?
4. If yes in Q. No.3 draw the circuit diagram.
5. Op-Amp as integrator or differentiator is a linear or non-linear application of Op-Amp. Comment.

EXPERIMENT NO.6

AIM OF THE EXPERIMENT: To study Schmitt Trigger using OP-AMP.

APPARATUS REQUIRED:

Sl.No.	Name of the apparatus	Specification	Quantity
1.	Analog Lab Trainer	Model DS-354	1
2.	Schmitt module kit	ADT-056	1
3.	DSO	DSO1052B, 50MHz, 1GSa/S	1
4.	Probes	T5060,60 MHz/6MHz, 10X:600Vpk, 1X:200Vpk, CAT-II	2
5.	Patch cords	4mm cords	As per requirement

CIRCUIT DIAGRAM:

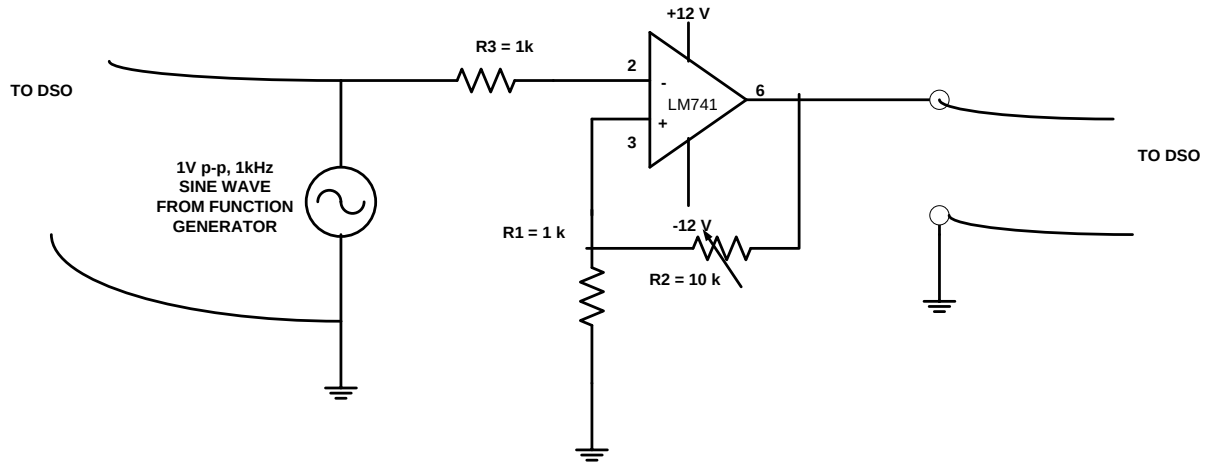

Fig. 6.1 Schmitt Trigger Circuit Using OP-AMP

THEORY: A Schmitt trigger circuit is also called a regenerative comparator circuit. The circuit is designed with a positive feedback and hence will have a regenerative action which will make the output switch levels. Also, the use of positive voltage feedback instead of a negative feedback, aids the feedback voltage to the input voltage, instead of opposing it. The use of a regenerative

circuit is to remove the difficulties in a zero-crossing detector circuit due to low frequency signals and input noise voltages. Shown below is the circuit diagram of a Schmitt trigger. It is basically an inverting comparator circuit with a positive feedback. The purpose of the Schmitt trigger is to convert any regular or irregular shaped input waveform into a square wave output voltage or pulse. Thus, it can also be called a squaring circuit. As shown in the circuit diagram, a voltage divider with resistors Rdiv1 and Rdiv2 is set in the positive feedback of the 741 IC op-amp. The same values of Rdiv1 and Rdiv2 are used to get the resistance value Rpar = Rdiv1||Rdiv2 which is connected in series with the input voltage. Rpar is used to minimize the offset problems. The voltage across R1 is fed back to the non-inverting input. The input voltage Vi triggers or changes the state of output Vout every time it exceeds its voltage levels above a certain threshold value called Upper Threshold Voltage (Vupt) and Lower Threshold Voltage (Vlpt). Let us assume that the inverting input voltage has a slight positive value. This will cause a negative value in the output. This negative voltage is fed back to the non-inverting terminal (+) of the op-amp through the voltage divider. Thus, the value of the negative voltage that is fed back to the positive terminal becomes higher. The value of the negative voltage becomes again higher until the circuit is driven into negative saturation (-Vsat). Now, let us assume that the inverting input voltage has a slight negative value. This will cause a positive value in the output. This positive voltage is fed back to the non-inverting terminal (+) of the op-amp through the voltage divider. Thus, the value of the positive voltage that is fed back to the positive terminal becomes higher. The value of the positive voltage becomes again higher until the circuit is driven into positive saturation (+Vsat). This is why the circuit is also named a regenerative comparator circuit.

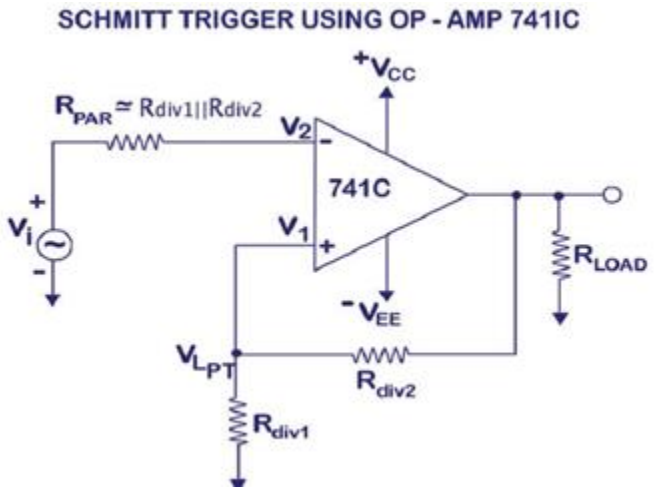

Fig. 6.2 Schmitt Trigger Circuit Using OP-AMP

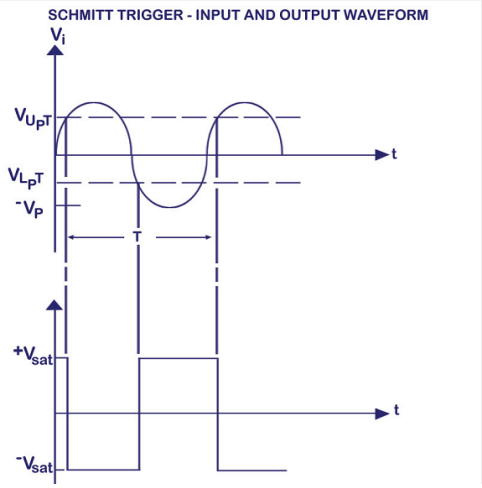

Fig. 6.3 Output of Schmitt Trigger Circuit Using OP-AMP

When Vout = +Vsat, the voltage across Rdiv1 is called Upper Threshold Voltage (V_{upt}). The input voltage, Vin must be slightly more positive than V_{upt} in order to cause the output Vo to switch from +Vsat to -Vsat. When the input voltage is less than V_{upt}, the output voltage Vout is at +Vsat. Upper Threshold Voltage, V_{upt} = +Vsat (Rdiv1/[Rdiv1+Rdiv2]) When Vout = -Vsat, the voltage across Rdiv1 is called Lower Threshold Voltage (V_{lpt}). The input voltage, Vin must be slightly more negative than V_{lpt} in order to cause the output Vo to switch from -Vsat to +Vsat. When the input voltage is less than Vlpt, the output voltage Vout is at -Vsat. Lower Threshold Voltage, Vlpt = -Vsat (Rdiv1/[Rdiv1+Rdiv2]) If the value of V_{upt} and V_{lpt} are higher than the input noise voltage, the positive feedback will eliminate the false output transitions. With the help of positive feedback and its regenerative behavior, the output voltage will switch fast between the positive and negative saturation voltages. Since a comparator circuit with a positive feedback is used, a dead band condition hysteresis can occur in the output. When the input of the comparator has a value higher than V_{upt}, its output switches from +Vsat to -Vsat and reverts back to its original state, +Vsat, when the input value goes below V_{lpt}. This is shown in the figure below. The hysteresis voltage can be calculated as the difference between the upper and lower threshold voltages. $V_{hysteresis} = V_{upt} - V_{lpt}$ Substituting the values of V_{upt} and V_{lpt} from the above equations: $V_{hysteresis}$ = +Vsat (Rdiv1/Rdiv1+Rdiv2) – {-Vsat (Rdiv1/Rdiv1+Rdiv2)} $V_{hysteresis}$ = (Rdiv1/Rdiv1+Rdiv2) {+Vsat – (-Vsat)}

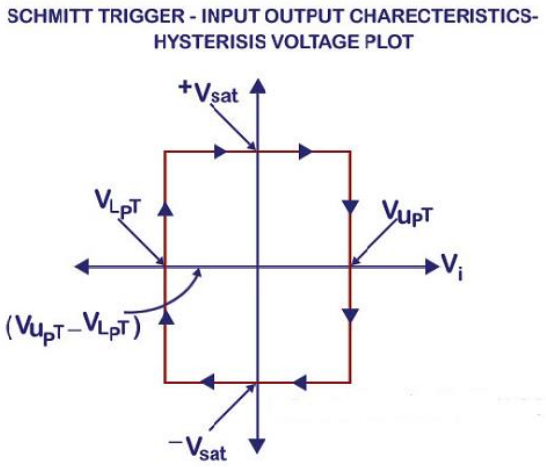

Fig. 6.3 Input-Output characteristics of Schmitt Trigger Circuit Using OP-AMP

PROCEDURE:

- Connect the circuit as per the circuit diagram.
- Set the function generator output for sine wave signal of amplitude at 1 V (p-p) and frequency 1 kHz.
- Set R_2 and R_3 values at fixed positions and note down the values in tabular form.
- Calculate theoretical values of V_{ut} and V_{lt} and note down the values in tabular form. ($+V_{sat}$ = +12 V, $-V_{sat}$ = -12 V.
- Apply the function generator output at input terminals V_i.
- Connect channel 1 and channel 2 of DSO to the input V_i and output V_0 respectively.
- Observe the square wave output on DSO for the given input sine wave and compare with sample wave form.
- Note down the practical V_{ut}, V_{lt} and V_H in tabular column.
- Compare the theoretical and practical values of V_{ut}, V_{lt} and V_H.

TABULATION:

Sl. No.	R_1 in Ω	R_2 in Ω	Theoretical Values			Practical Values		
			$V_{ut} = \frac{R_1}{R_1+R_2}(+V_{sat})$ in volts	$V_{lt} = \frac{R_1}{R_1+R_2}(-V_{sat})$ in volts	V_H in volts	V_{ut} in volts	V_{lt} in volts	V_H in volts

CONCLUSION:

DISCUSSION QUESTIONS:

1. Cite some applications of Schmitt Trigger.
2. Which feedback is used in Schmitt Trigger?
3. Schmitt Trigger is a linear or non-linear application of OP-AMP. (T/F)

EXPERIMENT NO.7

AIM OF THE EXPERIMENT: To study Transfer and Output characteristics of MOSFET.

APPARATUS REQUIRED:

Sl.No.	Name of the apparatus	Specification	Quantity
1.	Transistor Characteristics Module	Model DS-373	1
2.	Patch cords	4mm cords	As per requirement

CIRCUIT DIAGRAM:

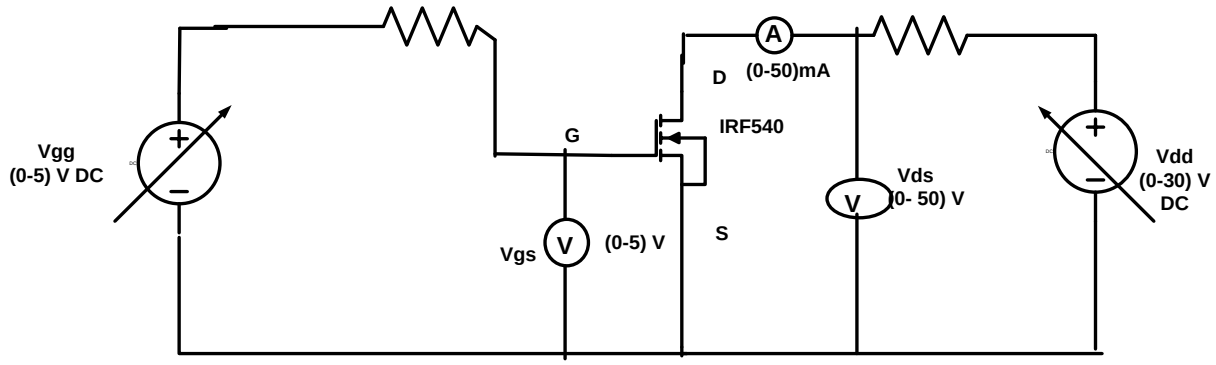

Fig. 7.1 n-Channel Enhancement type MOSFET

THEORY: Although there are some similarities in construction and mode of operation between depletion type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to source voltage reaches a specific magnitude. In particular, current control in an n-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for n-channel JFETs and n-channel depletion-type MOSFETs. If V_{GS} is set at 0 V and a voltage applied between the drain and the source of the device of the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively 0 A—quite different from the depletion-type MOSFET and JFET, where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and the source (due to the n-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p– n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source. Both

V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced n-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant increase in drain current is called the threshold voltage and is given the symbol V_T . On specification sheets it is referred to as V_{GS}(Th), although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with V_{GS} = 0 V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET. Both depletion- and enhancement type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

PROCEDURE:

Transfer Characteristics:

- Connect the circuit as per the circuit diagram.
- Get the connection checked by lab instructor or course instructor.
- Keep all the potentiometers in zero position.
- Set the drain to source voltage V_{DS}(0-30 V) to some constant voltage say 10 V.
- Slowly vary the gate voltage V_{GS} in steps of 0.2 V and note down the current I_D in mA.
- The device will get turn ON at some gate voltage V_{GS} which is called Threshold voltage V_{GST}.
- If $V_{GS} < V_{GST}$ small leakage current flows from drain to the source. If $V_{GS} > V_{GST}$ the drain current depends on the magnitude of gate voltage.
- As you find the turn on voltage of MOSFET, note down V_{GST} which varies from 2.5 V – 4 V.
- Take down the different reading of V_{GS} and I_D at different values of constant value of V_{DS}. Tabulate the reading for transfer characteristics.
- Plot the graph V_{GS} vs I_D shown below.

Output or Drain Characteristics:

- Connect the circuit as per the circuit diagram.
- Get the connection checked by lab instructor or course instructor.
- Keep all the potentiometers in zero position.
- Set the drain to source voltage V_{GS} to some constant voltage say 3 V.
- Slowly vary the gate voltage V_{DS} in steps of 0.2 V and note down the current I_D in mA.

- The device will get turn ON at some gate voltage V_{GS} which is called Threshold voltage V_{GST}.
- As you find the turn on voltage of MOSFET, note down V_{GST} which varies from 2.5 V – 4 V.
- Take down the different reading of V_{DS} and I_D at different values of constant value of V_{GS}. Tabulate the reading for transfer characteristics.
- Plot the graph V_{DS} vs I_D shown below.

TABULATION:

Transfer Characteristics:

Sl. No.	V_{DS} = 5.0 V		V_{DS} = 5.1 V		V_{DS} = 5.2 V	
	V_{GS} in Volts	I_D in mA	V_{GS} in Volts	I_D in mA	V_{GS} in Volts	I_D in mA
1.						
2.						
3.						
4.						
5.						
6.						
7.						
8.						
9.						
10.						

Output Characteristics:

Sl. No.	V_{GS} = 3V		V_{GS} = 3.1V		V_{GS} = 3.3V	
	V_{DS} in Volts	I_D in mA	V_{DS} in Volts	I_D in mA	V_{DS} in Volts	I_D in mA
1.						
2.						
3.						
4.						
5.						
6.						
7.						
8.						
9.						
10.						

MODEL GRAPH:

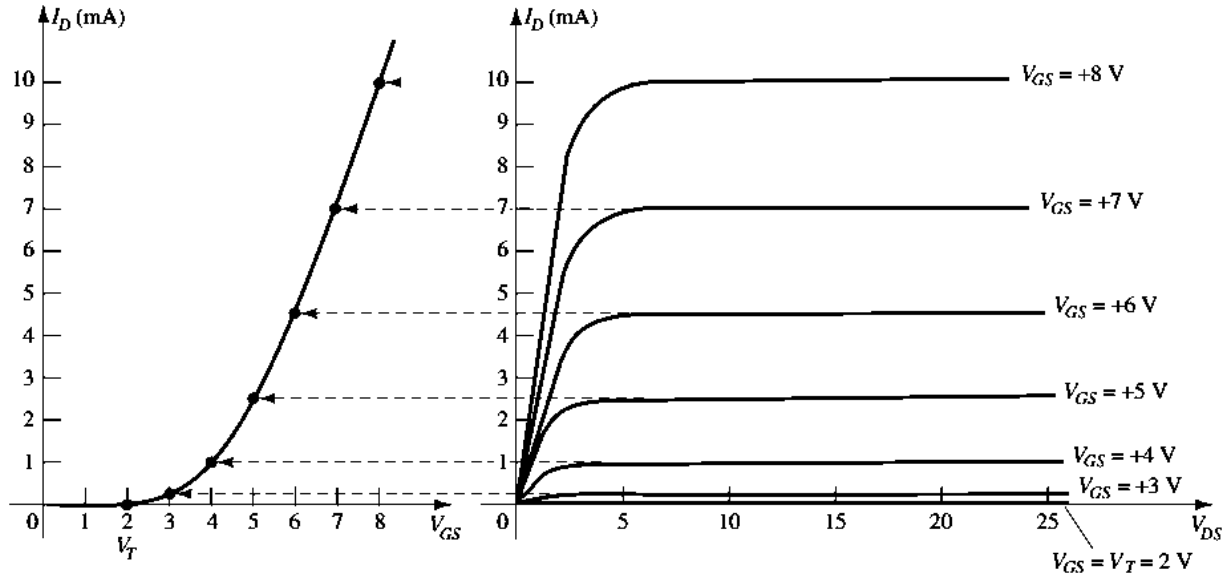

Fig. 7.2 Transfer and Output Characteristics of n-Channel Enhancement type MOSFET

CONCLUSION:

DISCUSSION QUESTIONS:

1. Explain trans conductance of MOSFET.
2. Explain Schockley's equation.
3. Cite two differences between enhancement and depletion type MOSFET.
4. MOSFET is a current controlled device. (T/F)
5. Cite one major differences between BJT and MOSFET.

EXPERIMENT NO.8

AIM OF THE EXPERIMENT: To study a-stable, mono stable and bi-stable multi-vibrator using 555IC timer.

APPARATUS REQUIRED:

Sl.No.	Name of the apparatus	Specification	Quantity
1.	Analog Lab Trainer	Model DS-354	1
2.	Astable Multivibrator Module	ALT-008	1
2.	Patch cords	4mm cords	As per requirement

CIRCUIT DIAGRAM:

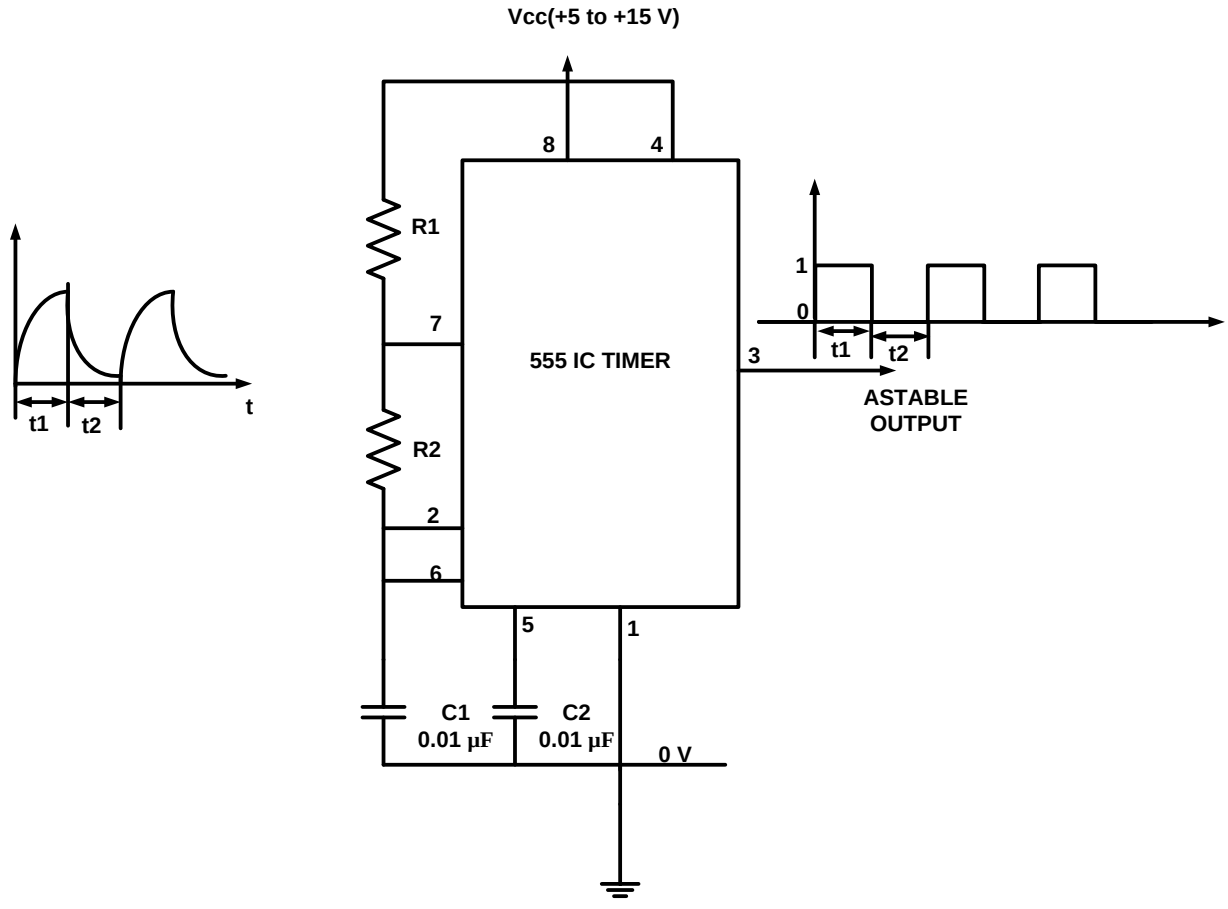

Fig. 8.1 Astable Operation of 555 IC timer

THEORY: Another popular analog–digital integrated circuit is the versatile 555 timers. The IC is made of a combination of linear comparators and digital flip-flops. The entire circuit is usually housed in an eight-pin package. A series connection of three resistors sets the reference voltage levels to the two comparators at $2V_{cc}/3$ and $V_{cc}/3$, the output of these comparators setting or resetting the flip-flop unit. The output of the flip-flop circuit is then brought out through an output amplifier stage. The flip-flop circuit also operates a transistor inside the IC, the transistor collector usually being driven low to discharge a timing capacitor. One popular application of the 555 timer IC is as an astable multivibrator or clock circuit. The following analysis of the operation of the 555 as an astable circuit includes details of the different parts of the unit and how the various inputs and outputs are used shows an astable circuit built using an external resistor and capacitor to set the timing interval of the output signal. Capacitor C charges toward V_{cc} through external resistors R_1 and R_2, we see that the capacitor voltage rises until it goes above $2V_{cc}/3$. This voltage is the threshold voltage at pin 6, which drives comparator 1 to trigger the flip-flop so that the output at pin 3 goes low. In addition, the discharge transistor is driven on, causing the output at pin 7 to discharge the capacitor through resistor R_2. The capacitor voltage then decreases until it drops below the trigger level ($V_{cc}/3$).The flip-flop is triggered so that the output goes back high and the discharge transistor is turned off, so that the capacitor can again charge through resistors R_1 and R_2 toward V_{cc}. The capacitor and output waveforms resulting from the astable circuit. Calculation of the time intervals during which the output is high and low can be made using the relations. On time $t_1 = 0.693\ (R_1+R_2)C$ and Off time $t_2 = 0.693\ R_2C$ and total time $T = t_1 + t_2$ and $f = 1/T$.

PROCEDURE:

- Connect the circuit as per the circuit diagram.
- Get the connection checked by lab instructor or course instructor.
- Switch on the power to the kit.
- In bistable mode state becomes high or low by the charging and discharging of capacitor.
- In mono stable mode there is only one stable state i.e low. If we press the pulse switch then after sometime the state is automatically low.
- Vary the potentiometer to vary the pulse width of output wave.
- Duty cycle is calculated using the formula given below.

CALCULATION:

Calculate the duty cycle by using the following formula

$t_1 = 0.693\ (R_1+R_2)\ C$

$t_2 = 0.693\ R_2C$

Duty ratio: $t_1 / (t_1 + t_2)$

CONCLUSION:

DISCUSSION QUESTIONS:

1. Cite some applications of 555 IC timer.
2. Give brief description about pin configuration of 555 IC timer.
3. Explain method of varying on time of pulse in astable multivibrator.
4. What is monostable multivibrator?
5. What is bistable multivibrator?