Dr. Jinti Hazarika

Assistant Professor
Department of Instrumentation Engineering
Jorhat Engineering College

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Career Objective

To advance academic and research excellence through innovative teaching and hands-on mentorship. Committed to fostering a dynamic learning environment, I aim to inspire students and cultivate critical thinking skills while actively engaging in cutting-edge research that contributes to the field of instrumentation and its applications.

Work Experience

Jorhat Engineering College

- *Assistant Professor* Sep. 2024 – Present
  - Appointed as an Assistant Professor in the Department of Instrumentation Engineering at Jorhat Engineering College, Assam, through the Assam Public Service Commission (APSC) by the Government of Assam.

Reliance New Solar Energy Limited

- *Manager* (Cell Process and Product Development) Apr. 2023 – Sep. 2024
  Responsibilities:
  - Led metallization paste and screen projects for cost reduction via qualification of new metallization paste suppliers and technologies.
  - Assess the performance and durability of metallization paste via reliability testing.
  - Analyze test data to identify potential failure modes and improve product quality.
  - Conduct risk assessments and prepare progress reports for stakeholders.
  - Prepare comprehensive reports on test outcomes and recommend improvements for product development.
  - Visit suppliers abroad to assess supplier capabilities, new metallization paste and screen technologies, ensuring alignment with quality and performance standards.
  - Coordinate with cross-functional teams and manage project timelines and budgets.
  - Stay updated on industry trends and advancements to integrate cutting-edge technologies into projects.

Indian Institute of Technology Roorkee, Uttarakhand, India

- *Junior Research Fellow* (sponsored by DRDO) Jul. 2015 - Oct. 2015
  Responsibilities: Designed a field-deployable signal processing system for measurement of path integrated gas concentration in real-time. Major duties included the generation of signals through an FPGA board using an analog circuit and MATLAB (DSP Builder) to drive the laser current, construction, and testing of an analog adder circuit to superimpose the signals. Visit DRDO laboratory, Delhi to present the results of the project.

Education

Indian Institute of Technology Guwahati, Assam, India

- **Ph.D.** 2024
  Thesis Topic: *"Design and Implementation of Hardware-Efficient Architectures for FFT Algorithms"*

Indian Institute of Technology Roorkee, Uttarakhand, India

- **M.Tech.** (Instrumentation and Signal Processing) 2015
  Thesis Topic: *"A Moving Window Filter Based Frequency Estimator for Capacitance Measurement"*

Jorhat Engineering College, Assam, India.

- **B.E.** (Instrumentation) 2012
  Project: *"Automatic Temperature Controlled Fan"*

Salt Brook Academy, Assam

- **HSSLC** (AHSEC, Science) 2008

Little Kingdom High School, Assam

- **HSLC**, (SEBA) 2006

Skills Set

- **Simulation Tools**: MATLAB, DSP Builder.
- **Languages**: Verilog, Latex (scripting language)
- **Typesetting Tools**: Texmaker, Microsoft Office Tools, Microsoft Visio, IPE
- **Synthesis Tools**: Synopsis Design Compiler
- **Hardware Kits**: Xilinx FPGAs, Intel (Altera) FPGAs

Research Interests

Digital Signal Processing Algorithms and Architectures.

Teaching Experience

- Teaching Assistant at IIT Guwahati
- Teaching Assistant at IIT Roorkee
- Teaching Assistant at NPTEL (Microprocessors and Interfacing, System Design through Verilog)

Projects

- **Indian Institute of Technology Roorkee**
  Moving Window Filter based Frequency Estimator for Capacitance Measurement Jun. 2014-Apr. 2015
  Objective: To design a capacitance measurement technique based on frequency estimator and moving window filter and simulation of this model using Matlab (DSP Builder) and to implement it in hardware.

- **Jorhat Engineering College**
  Analogue Capacitance Meter Feb. 2012- Jun. 2012
  Developed a model for measuring capacitance of unknown capacitors. Experiments were performed to study the characteristic relation between capacitance and current.

- **Jorhat Engineering College**
  Automatic Temperature Controlled Fan Aug. 2011- Dec. 2011
  Designed a model for controlling the speed of a fan automatically by monitoring the environmental changes detected by the temperature sensor.

- **Jorhat Engineering College**
  Invisible Intruder Alarm Oct. 2010 - Dec. 2010
  Implemented an ultra compact intruder alarm system based on the detection of an intrusion caused by the interruption of an infra-red light beam being emitted by an infra-red LED and falling on matched photo diode.

- **Jorhat Engineering College**
  Sound Operated Intruder Alarm Aug. 2010 - Oct. 2010
  Implemented a circuit as a burglar alarm that operates automatically by picking up sounds and provides both flashing light and an intermittent audio tone indication.

Professional Membership	*IEEE* Student Member	Mar. 2018–Present
	IEEE Circuits and Systems Society (CASS) Member	Mar. 2018–Present

Publications

1. M.T. Khan and **J. Hazarika**, "An Area and Energy Efficient Serial-Multiplier", *IEEE Embedded Systems Letters*, Jan. 2024. [DOI: 10.1109/LES.2024.3352540]
2. **J. Hazarika**, M.T. Khan, S. R. Ahamed and H. B. Nemade, "An Efficient Implementation Approach to FFT Processor for Spectral Analysis", *IEEE Transactions on Instrumentation and Measurement*, Aug. 2023. [DOI: 10.1109/TIM.2023.3301891]
3. M. A. Alhartomi, M. T. Khan, S. Alzahrani, A. Ahmed, S. R. Ahamed, **J. Hazarika**, R. Alsulami, A. Alotaibi and M. Al-Harthis, "Low-Area and Low-Power VLSI Architectures for Long Short-Term Memory Networks", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Jan. 2023. [DOI: 10.1109/JETCAS.2023.3330428]
4. **J. Hazarika**, R. A. Shaik and H. B. Nemade, "Low-complexity, Energy-Efficient Fully-Parallel Split-Radix FFT Architecture", *IET Electronics Letters*, Jun. 2022. [DOI: 10.1049/ell2.12565]
5. R. K. Sharma, M. T. Khan, R. A. Shaik and **J. Hazarika**, "Novel Time-shared and LUT-less Pipelined Architecture for LMS Adaptive Filter", *IEEE Transactions on VLSI System*, Sep. 2019. [DOI: 10.1109/TVLSI.2019.2935399]
6. **J. Hazarika**, M. T. Khan, R. A. Shaik and H.B. Nemade, "Energy Efficient VLSI Architecture of Real-Valued Serial Pipelined FFT", *IET Computers and Digital Techniques*, Jun. 2019. [DOI: 10.1049/iet-cdt.2019.0025]
7. **J. Hazarika** and P. Sumathi, "Moving Window Filter Based Frequency-Locked Loop for Capacitance Measurement", *IEEE Transactions on Industrial Electronics*, Dec. 2015. [DOI: 10.1109/TIE.2015.2459051]

Conference Publications

1. **J. Hazarika**, M. T. Khan, R.A. Shaik and H.B. Nemade, "An Area and Power Efficient Serial Commutator FFT with Recursive LUT Multiplier", *International conference on Modelling, Simulation and Intelligent Computing (MoSICom) 2020, Springer*, Dubai, UAE.
2. **J. Hazarika**, M. T. Khan, R.A. Shaik and H.B. Nemade, "High Performance Multiplierless Serial Pipelined VLSI Architecture for Real-Valued FFT", *25th National Conference on Communication (NCC), Feb. 2019, IEEE, IISc Bengaluru.* [**Nominated for Best Paper Award**]
3. **J. Hazarika**, M. T. Khan and R.A. Shaik, "Low-Complexity Continuous-Flow Memory-Based FFT Architectures for Real-Valued Signals", *2019 32nd International Conference on VLSI Design and 18th International Conference on Embedded Systems (VLSID), Jan. 2019, IEEE, Delhi.* [**Best Student Paper Award**]

Positions/ Recognitions

- **Reviewer**, *IEEE Transaction on Circuits and Systems I, II* (TCAS I, TCAS II), *IEEE Transaction on VLSI System* (TVLSI), *Springer Circuits, Systems and Signal Processing* (CSSP), *Elsevier Computers and Electrical Engineering*, *International Symposium on Circuits and Systems* (ISCAS), MWSCAS.
- **Head Teaching Assistant (TA) Coordinator** for a subject, EEE Dept., IIT Guwahati July. 2019 – Jan. 2020
  Course consisted of 24 faculties, 40 TAs and 900+ students.
- **Webpage Coordinator**, EEE Dept., IIT Guwahati Nov. 2020 – Feb. 2021

Scholarships /Awards

- *Best Student Paper Award* of 35000 INR in VLSID-2019. Jan. 2019
- *Fellowship Award* of 6000 INR in VLSID-2019. Jan. 2019
- *Scored* 90.91 percentile in GATE 2012. Mar. 2012
- One time amount of 1 Lakh INR received under *Chief Minister's Scheme for Financial Assistance to Meritorious Students of Assam*.
- *Oil India Limited Merit Scholarship* received in honour and recognition of my performance in High School Leaving Certificate Examination, 2006.
- *Anundoram Borooah Award* received from the Chief Minister of Assam for recognition of excellent academic performance in securing first division with star marks in High School Leaving Certificate Examination, 2006.